AMENDMENTS TO THE CLAIMS

1. (Original) A data processing system, comprising:

at least one function module connected to a single system bus;

a data transfer controller which outputs a first bus use permission request signal based on a data transfer request signal output from the at least one function module;

a central processing unit connected to the system bus which outputs a second bus use permission request signal;

an arbitration controller for determining, based on the first and second bus use permission request signals, which of the data transfer controller and the central processing unit should obtain a permission to use the system bus;

a section for setting a first data amount which can be continuously transferred by the at least one function module;

a section for suspending an output of the first bus use permission request signal to the arbitration controller for at least one clock cycle after a data transfer by the at least one function module is completed; and

a section for giving the permission to use the system bus to one of the data transfer controller and the central processing unit in such a manner that the data transfer controller has a priority over the central processing unit during a period when the first bus use permission request signal is being issued.

Claim 2 (Cancelled).

3. (Original) A data processing system according to claim 1, wherein, after a data transfer by the at least one function module is completed and the output of the first bus use permission request signal to the arbitration controller is then suspended for at least one clock cycle, in the case where the output of the first bus use permission request signal to the arbitration controller is further suspended for another one or more clock cycles, the permission to use the system bus is given to the central processing unit based on the second bus use permission request signal.

4. (Original) A data processing system according to claim 1, further including a section for setting a second data amount which can be continuously transferred by the central processing unit,

wherein in the case where the second data amount is not equal to a predetermined amount, the central processing unit continues to execute data transfer even when the data transfer controller is requesting the permission to use the system bus during the data transfer by the central processing unit.

5. (Original) A semiconductor device including the data processing system of claim 1.

6. (Original) A digital camera apparatus including the semiconductor device of claim 5.

7. (Currently amended) A semiconductor device including the data processing system of ~~claim 2~~ claim 13.

8. (Original) A digital camera apparatus including the semiconductor device of claim 7.

9. (Original) A semiconductor device including the data processing system of claim 3.

10. (Original) A digital camera apparatus including the semiconductor device of claim 9.

11. (Original) A semiconductor device including the data processing system of claim 4.

12. (Original) A digital camera apparatus including the semiconductor device of claim 11.

13. (New) A data processing system, comprising:

at least one function module having a first priority connected to a single system bus;

a data transfer controller outputting a first bus use permission request signal based on a

data transfer request signal output from the at least one function module;

a central processing unit connected to the system bus which outputs a second bus use permission request signal;

an arbitration controller for determining, based on the first and second bus use permission request signals, whether the data transfer controller or the central processing unit should obtain a permission to use the system bus;

a first section for setting a first data amount which can be continuously transferred by the at least one function module;

a second section for selectively suspending an output of the first bus use permission request signal to the arbitration controller for at least one clock cycle after a data transfer by the at least one function module is completed unless a data transfer request signal is being issued by the at least one function module and the priority of the at least one function module issuing the data transfer request is higher than a priority of the central processing unit; and

a third second for giving the permission to use the system bus to one of the data transfer controller and the central processing unit in such a manner that the data transfer controller has a priority over the central processing unit during a period when the first bus use permission request signal is being issued.

14. (New) A method of processing data comprising the steps of:

connecting at least one function module to a single system bus;

providing a data transfer controller;

outputting a data transfer request signal from the at least one function module to the data transfer controller;

providing an arbitration controller;

outputting from the data transfer controller to the arbitration controller a first bus use permission request signal based on the data transfer request signal output from the at least one function module;

connecting a central processing unit to the system bus;

outputting a second bus use permission request signal from the central processing unit to

the arbitration controller;

determining, based on the first and second bus use permission request signals, which of the data transfer controller and the central processing unit should obtain a permission to use the system bus;

setting a first data amount which can be continuously transferred by the at least one function module;

suspending the first bus use permission request signal to the arbitration controller for at least one clock cycle after a data transfer by the at least one function module is completed; and

giving the permission to use the system bus to one of the data transfer controller and the central processing unit in such a manner that the data transfer controller has a priority over the central processing unit during a period when the first bus use permission request signal is being issued.